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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,430	10/29/2003	Min-Hwa Chi	TS00-680B	6774

7590 06/03/2004

George O. Saile
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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,430	CHI, MIN-HWA	
	Examin r	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24 and 26-32* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In the Preliminary Amendment dated October 29, 2003, Applicant has amended the specification and canceled claims **1-23** is acknowledged. Accordingly, claims **24-32** are pending in the application, which is a division of Application No. 10/056,622 filed 01/28/2002, U.S. Patent No. 6,657,240.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on January 29, 2004. The references cited on the PTOL 1449 form have been considered.

Claim Objections

Claims **1 and 29** are objected to because of the following reasons.

In claim **1**, the "BIT" in the "... BIT transit time diode device ..." should read –BBT--.

In claim **29**, the "said said emitter" should read –said emitter--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **24, 26-28 and 31-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebina (USP: 6,734,500) in view of Finney (USP: 6,404,037).

Regarding claim **24**, Ebina discloses in Figs. 1, 4-6, and 8-13, and related texts as set forth in column 9, line 55-column 12, line 41, a method for manufacturing a semiconductor device comprises:

providing a semiconductor layer (10a) in a SOI substrate (10);

implanting ions into said semiconductor layer to form an emitter region (210) (Fig. 6, col. 10, lines 45-50);

implanting ions into said semiconductor layer to form a barrier region/a base region (220) (Fig. 6, col. 10, lines 51-56);

forming an insulator layer/a gate dielectric layer (140) overlying said semiconductor layer (Fig. 4, col. 10, line 11);

depositing a conductor layer/a polysilicon layer (60, 70, 110) overlying said insulator layer (Fig. 10, col. 12, lines 14-19);

patterning said conductor layer/the polysilicon layer to form a gate (60, 70, 110) wherein said gate overlies said barrier region (Figs. 6 and 10); and

thereafter implanting ions into said semiconductor layer to form a collector region (230) (Figs. 6 and 13, col. 12, lines 34-39) and to complete said diode device in the manufacture of said integrated circuit device wherein a drift region/a body region (52a) (Fig. 6, col. 10, line 5) is formed in said semiconductor layer where said gate overlies said semiconductor layer between said collector region and said barrier region.

Ebina fails to teach or suggest a method for manufacturing a semiconductor device comprises wherein said gate overlies at least part of said emitter region.

Finney teaches in Fig. 1 and related text an insulated gate bipolar transistor comprises a gate portion (10) which is formed and includes a conductive gate electrode (11) and a thin insulating layer (12) and which extends substantially across a part of the emitter region (6) in such a way as to enable an inversion channel (13) to be formed across the emitter region between the further region (8) and the base portion (4) as set forth in column 2, lines 3-9.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a gate overlying a part of the emitter region, as taught by Finney to incorporate into Ebina's teachings to arrive the claimed limitation in order to form an inversion channel and to improve reverse bias conducting properties of the device (col. 1, lines 6-9).

Regarding claim **26**, Ebina discloses the method according to Claim **24** wherein said semiconductor layer comprises silicon (col. 16, line 31).

Regarding claim **27**, Ebina discloses in Figs. 4-6, the method according to Claim **24** further comprising forming a buried insulator layer/an insulation layer (10b) overlying said substrate prior to said step providing a semiconductor layer overlying said substrate (col. 9, lines 55-58).

Regarding claim **28**, Ebina discloses in Figs. 4-6, the method according to Claim **24** wherein said semiconductor layer (10a) comprises one of the group of: n-type doped and p-type doped.

Regarding claim **31**, Ebina discloses the method according to Claim **24** wherein said conductor layer consists of one of the group of: polysilicon, metals, metal silicide, metal nitrides, and combinations thereof (col. 12, lines 14-19).

Regarding claim **32**, Ebina discloses the method according to Claim **24** wherein said insulator layer consists of one of the group of: oxide, silicon oxide, silicon oxynitride, silicon nitride, tantalum oxide, and aluminum oxide (col. 14, line 58-59).

Claims **29 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebina (USP: 6,734,500) in view of Finney (USP: 6,404,037) and further in view of Fig. 1 Prior Art.

Ebina and Finney disclose the claimed limitation except for the method according to Claim **24** wherein said emitter region is n-type/p-type, said barrier region is p-type/n-type, and said collector region is p-type/n-type. Fig.1 Prior Art teaches that the IMPATT device comprises semiconductor bulk regions (14, 18, 22, and 26). This semiconductor bulk region comprises a source region (14, n+), a barrier region (18, p), a drift region (22), and a collector region (26, p+). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the emitter region being n-type or p-type, the barrier region being p-type or n-type, and the collector region being p-type or n-type since it was known in the art that is typical dopant profile for the "negative resistance" diodes (Description of the Prior Art).

Allowable Subject Matter

Claim **25** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations.

Ebina and Finney, taken alone or in combination, fail to teach the claimed limitation the method according to Claim **24** wherein said step of implanting ions into said semiconductor layer to form an emitter region comprises arsenic ions, wherein said step of implanting ions into said semiconductor layer to form a barrier region comprises boron ions, and wherein each of said steps are performed using common masking layer and a common annealing process.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

AH

May 27, 2004

Andy Huynh

Patent Examiner